A 53 GHz DCO for mm-Wave WPAN

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Abstract— A digitally-controlled oscillator (DCO) for mm-wave wireless applications is demonstrated for the first time. Low phase noise is achieved adopting an efficient complementary topology and optimizing the programmable-capacitor array. A fine frequency resolution of 1.8MHz is obtained using switched metal-oxide-metal capacitors while coarse frequency tuning is achieved using switched accumulation-mode MOS varactors. The DCO, implemented in 90nm CMOS technology, has a power consumption of 2.34 mW, an oscillation frequency ranging from 51.3 to 53.3 GHz, and a measured phase noise of -116.5 dBc/Hz at 10MHz from the carrier, with a resulting figure-of-merit equal to -187.2 dBc/Hz.

I. INTRODUCTION

The ongoing progress in CMOS technology and circuit design research is opening the way to highly-integrated low-cost wireless systems working in the millimeter-wave frequency range [1][2]. One of the possible applications are wireless networks, that, thanks to the widespread success of WLAN systems and the ever growing demand for higher data-rate communications, are leading to increasing congestion in the frequency bands below 10 GHz. The 7-GHz unlicensed band around 60 GHz offers the possibility of proving short-range wireless data communications at rates of several gigabits per second and is therefore being subject of intensive research. Thanks to the reduced wave-length, the antenna has a reasonable size that allows it to be integrated with a complete radio on the same chip [3], reaching unprecedented levels of integration. Such an ambitious goal presents many design challenges mainly because of the high operative frequencies and the low analog qualities of MOS transistors in deep-submicron CMOS technologies, supporting the use of a digitally intensive design approach. In this paper, a low phase noise digitally-controlled oscillator (DCO) for high performance mm-wave wireless personal area network transceivers is presented. The oscillator was designed in a 90nm CMOS process without advanced analog features and adopts a fully-digital control technique, making it compatible with all-digital frequency synthesis. In section II the oscillator digital tuning circuitry is described; section III and IV report on the oscillator design and experimental characterization; section V draws some conclusion.

II. DIGITALLY CONTROLLED CAPACITOR BANK DESIGN

In a DCO the variable capacitance consists in an array of digitally-controlled capacitors where the total variable capacitance and the minimum capacitance step are determined by the desired tuning range and by phase noise considerations. Modeling the DCO frequency quantization as a uniformly-distributed random variable [4], its effect on phase noise, or frequency quantization noise (FQN), is theoretically given by:

\[ PN(f) = \left( \frac{f_{\text{LSB}}}{f} \right)^2 \frac{T_{\text{REF}}}{12} \left( \sin \frac{\omega}{T_{\text{REF}}} \right)^2 \]

where \( T_{\text{REF}} \) is the PLL reference frequency, \( f_{\text{LSB}} \) is the frequency resolution of the DCO and \( f \) is the frequency offset from the carrier. Assuming \( f_{\text{LSB}} \) equal to 2MHz and 20 ns \( T_{\text{REF}} \), a FQN of -102.3 dBc/Hz at 10MHz offset from the carrier results, which is higher than what can be achieved in terms of thermal-induced phase noise at reasonable power levels. The FQN can be lowered further using \( \Sigma \Delta \) noise-shaping techniques as proposed in [4]. For instance, using a 2\(^{nd}\)-order \( \Sigma \Delta \) modulation at 500MHz, FQN for the same \( f_{\text{LSB}} \) would be lowered to -147.8 dBc/Hz at 10MHz from the carrier. A target \( f_{\text{LSB}} \) of 2MHz has been assumed in this work.

One of the major shortcomings in the implementation of LC-tank oscillators above 10GHz is the low quality factor (Q) of the capacitors, that usually dominates the overall Q of the resonator. This is even more true for variable capacitors, both MOS varactors and switched Metal-oxide-Metal (MoM) capacitors, where additional losses are brought about by active device limitations (gate resistance, finite channel conductance and parasitic drain/source capacitance). To better cope with technology limitations at high frequencies, as opposite to a previous implementation at 10-GHz [5], the capacitor bank was segmented into three sections, implemented with different structures. Tuning range and Q are the primary drivers for the coarse tuning bank, while small minimum capacitance step is the main requirement for the fine tuning bank. Segmentation also allows to reduce the overall size of the capacitor arrays compared to a uniform array of equal resolution, minimizing the parasitic inductances that would hinder oscillation at 50GHz. The coarse and intermediate sections are intended to be used in the initial phase of the locking algorithm, similarly to what is done in analog PLLs when the VCOs uses switched tuning, while the fine tuning bank is used in the normal operation of the PLL. For the coarse tuning section, two different tuning devices have been considered in this work: the NMOS in n-well accumulation-mode (a-MOS) varactor, switched between the extremes of its C-V characteristic, and the NMOS transistor operated as a switch [6]. To compare the two devices, a variable-capacitance figure of merit (FoM\(_C\)) has been used:

\[ \text{FoM}_C = \frac{1}{\omega_0 R_{\text{ON}} C_{\text{off}}} \]

where \( \omega_0 \) is the oscillation frequency, \( R_{\text{ON}} \) is the resistance of the device when it exhibits the maximum value of capacitance.
(corresponding to the accumulation region for the varactor) while $C_{\text{off}}$ is the minimum capacitance. In this both quality factor and tuning capability ($C_{\text{max}}/C_{\text{min}}$) are taken into account. At the time of design, a scalable model of the a-MOS varactors was not available in the technology design kit. Based on the device model of an a-MOS varactor with fixed device size (finger width of 1.6 $\mu$m, channel length of 400 nm), a custom Verilog-A scalable model has been developed using simplified device equations [7]. Based on this approximate varactor model and on the switch device model, a comparison of the two structures has been carried out for different device sizes. Depending on the chosen channel length ($L_f$) and finger width ($W_f$), the a-MOS varactor or the switched-MoM capacitor features an higher FoM. At $W_f=1\mu$m and $L_f=100\text{nm}$ the a-MOS varactor reaches the maximum FoM, equal to 128 at 50 GHz, that is approximately three times greater than the MOS switch’s maximum one, even neglecting the bottom-plate capacitance of the latter. Hence, an a-MOS varactor was used for the coarse tuning section, while custom-designed MoM capacitors were used to achieve a finer frequency resolution than would be attainable using a minimum-sized a-MOS varactor. The coarse tuning bank is formed by 31 identical a-MOS, controlled by a 5-bit binary word. According to the approximate model this should cover a frequency range of about 3.2 GHz with a frequency resolution equal to 104 MHz. The fine tuning bank is formed by 31 MoM capacitors with series MOS switches controlled by a 5-bit thermometer code to ensure monotonicity. The physical implementation of two adjacent elements is shown in Fig. 1. A single top layer (M6) is used for all capacitors while the bottom layer of each capacitor unit is implemented as a metal stack (M4-M1) connecting to the NMOS transistor switch.

\[
C_{\text{off}} = 2 \left( \frac{\varepsilon_{\text{ox}} \cdot C_{\text{ox}}}{C_{\text{off}} + \varepsilon_{\text{ox}} \cdot C_{\text{ox}}} + C_{\text{ox}} \right)
\]

In order to obtain the desired frequency resolution of about 2 MHz, an LSB capacitance step in the order of 10 aF is required. This has been achieved using a small MoM capacitor with a top-bottom capacitance in the order of 60 aF, a bottom-ground capacitance of about 80 aF and a minimum-sized switch in series. The actual capacitance variation, taking into account the finite on-resistance and the parasitic capacitance introduced by the switch is given by the expression in Fig. 1. The unavoidable coupling between adjacent cells determines a non-linearity in the code-to-frequency characteristic. The sizing of each plate and the distance between two adjacent plates have been optimized using EMX electromagnetic simulator. According to electromagnetic simulations, the error caused by the capacitive coupling between adjacent elements of the bank is lower than 1/9 LSB. Extending the tuning range of the fine-tuning section up to the frequency resolution of the coarse-tuning section with some margin would require more than 100 elements, resulting in an exceedingly large structure. To bridge the gap between the coarse and fine tuning elements, an intermediate tuning bank has been added. The intermediate tuning bank is made of 7 MoM capacitors with series MOS switches controlled by a 3-bit binary word.

### III. Oscillator Design

In Fig. 2 the DCO schematic is illustrated. The core consists of a complementary NMOS-PMOS cross-coupled pair that generates the negative resistance required to sustain oscillation. The use of a complementary topology allows to achieve near double current efficiency as compared to the single-pair topology, enhancing the oscillator efficiency while keeping the low-voltage transistors, including the a-MOS varactors, always below $V_{\text{DD}}$. Furthermore, with the a-MOS gates biased around $V_{\text{DD}}/2$ and a rail-to-rail voltage swing, close to maximum tuning of the varactors is achieved without requiring the control voltage, connected to the a-MOS source/drain terminals, to swing above $V_{\text{DD}}$.

The core transistors have been sized according to the main targets of minimizing phase noise and complying with the oscillation start-up condition with some margin ($\varepsilon R_{\text{TANK}}=3$) while taking into account layout-related parasitics. For a given total device width, reducing the finger width helps lowering gate resistance but increases device perimeter and interconnect parasitic capacitances. The use of a complementary pair introduces an additional degree of freedom in the design and layout of the transistors. In order to minimize layout parasitics, PMOS and NMOS transistors were laid out with the same number of fingers. The finger widths have been chosen in order to optimize the $f_{\text{MAX}}$ of the pair. The expected overall fixed capacitance contributed by the active devices, including interconnect parasitics, is
approximately 90 fF. In order to minimize parasitic series
inductances, the coarse tuning varactors were laid out right
beside the active devices, as shown in Fig. 3. The single-turn
inductor, physically implemented on the top metal layer (M6),
has been optimized for maximum Q and to facilitate the
placement of active core and capacitor arrays. An accurate
inductor circuit model, which is of primary importance for
accurate simulations, has been derived from Agilent-
Momentum EM simulations. The inductor layout and its
circuit double-π model [8], valid in the range 50-70GHz, are
reported in Fig. 3. Inductance value is about 70 pH, with a
differential Q of 19 at 60 GHz.

### IV. Experimental Results

The test chip has been designed and implemented in TSMC
90nm CMOS process with 6 levels of metal and ultra thick top
metal. A chip micrograph is reported in Fig. 4. Bias and
control pads are located on the top (not showed) while the two
outputs, suitable for on-chip measurement with GSG probes,
are in the lower portion. The chip, including all pads,
measures 1078 x 760 µm$^2$, but most of the chip area is
occupied by the output buffer, which is only required for
testing purposes. The core circuit area is only 106 x 83 µm$^2$.

The measurement setup for the DCO characterization is
reported in Fig. 5. The oscillator was characterized on-chip by
directly probing its output in single-ended configuration. The
outgoing signal from the probes is down-converted by means
of a Wisewave V-band mixer, driven by a 51-53GHz local-
oscillator provided by an Agilent E8527D generator. In order
to improve phase noise measurement accuracy, an
intermediate-frequency amplifier on a custom-made board is
used to boost the signal level. Phase noise is finally measured
using an R&S FSUP signal analyzer using the cross-
correlation method. The lack of the tail current generator in
this design makes the oscillator more sensitive to disturbances
on the power supply. This has been addressed during testing
using two separate boards: one small-sized microwave board
where the chip is down-bonded and large bypass capacitors
are used to heavily filter the supply and control lines; one
larger control board that is used to generate and process the
control signals.

The oscillation frequency as a function of the coarse tuning
5-bit binary control word is given in Fig. 6. The measured
tuning range of 2 GHz, is lower than predicted probably due
to underestimation of the minimum depletion capacitance of
the a-MOS varactor by the approximate model used in this
work. The average frequency step is 64 MHz, with less than
50-MHz differential non-linearity (DNL). The intermediate
tuning section shows a tuning range of 102 MHz, an average
frequency step of 14 MHz and a DNL of less than 3 MHz. The
frequency range covered by the fine tuning section is 54 MHz,
with an average step of 1.8 MHz. Accurate direct
measurements of the individual fine frequency steps were not
possible using the aforementioned setup. Therefore, an
indirect measurement has been carried out taking advantage of
the thermometer-code control to toggle a single capacitor at a
time, performing a narrow-band digital frequency modulation.
This results in a pair of sidebands around the carrier with
relative amplitudes proportional to the frequency step that can
be easily measured using the spectrum analyzer. The
modulating frequency must be chosen carefully in order to
minimize unwanted effects due to on-board parasitics on the
ground and control lines, and such that the narrow-band
assumption is satisfied. A modulating frequency between 30-
40MHz has been chosen. Due to an implementation mistake in
the control board only a sub-set of the fine-tuning capacitors
could be tested. The measured frequency step is equal on
average to 1.78 MHz, consistently with the direct
measurement carried out between the extremes of the tuning
code, with a maximum deviation of 200 kHz.
V. CONCLUSIONS

A low phase-noise digitally-controlled oscillator suitable for millimeter-wave wireless applications has been proposed and demonstrated for the first time in this paper. The circuit, implemented in a digital 90nm CMOS process, shows very good efficiency and enables to employ fully digital frequency control in the frequency synthesizer.

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