

Efficient Full-Wave Simulation in Layered, Lossy Media

Sharad Kapur* David E. Long* Jinsong Zhao†

* Bell Laboratories, Lucent Technologies, Murray Hill, NJ 07974

† University of California, Santa Cruz, CA 95064

Abstract

We describe a fast integral equation-based method for full-wave extraction in layered media. The method uses a combination of the fast integral equation solver IES³, layered Green’s functions, and a formulation that gives a well-conditioned linear system even in the “electrically-small” regime (i.e., when circuit structures are a fraction of the wavelength of light). The overall approach gives $O(N \log N)$ complexity, where N is the number of panels in a discretization of the conductor surfaces. We apply our method to the simulation of an integrated inductor on a lossy CMOS substrate and compare the results to measurement.

I. Introduction

Extraction and simulation of passive components play a significant role in the design of modern RF ICs. Increasing frequencies have made “full-wave” simulation critical for components that may be operated near resonance. General purpose field solvers based on finite-difference or finite-element schemes (e.g., Ansoft and HP-HFSS) can be used. However, they require volume discretization, resulting in large computation time and memory use, and it is difficult to enforce radiating boundary conditions for open regions. Simulation tools based on layered media integral equation formulations (such as HP-Momentum and Sonnet) are popular in the microwave and antenna communities. However, these tools employ direct solution methods which restricts them to small problems. In addition, the formulations that they are based on become ill-conditioned at lower frequencies, resulting in numeric difficulties. More recently, an integral equation formulation was combined with the pre-corrected FFT method for the efficient solution of electromagnetic problems [9]. While the algorithm is fast, it is likely to be applicable only to electrically large structures. More importantly, since it has not been combined with a layered media Green’s function, it does not capture dielectric variation in the layers and loss in the substrate.

In this paper we present a general purpose full-wave electromagnetic analysis tool for the rapid simulation of passive structures in layered, lossy media. An integral equation formulation is used whereby all layered effects are captured by Green’s functions [7], [8], [14]. A Galerkin-like scheme is used with basis functions that are composed of linear subsectional rooftop functions [10]. Ill-conditioning at low frequencies is avoided by choosing an appropriate mix of curl-free and divergence-free basis functions. The good conditioning, together with the fact that typical Green’s functions vary smoothly with distance, are exploited us-

ing the fast integral equation solver IES³ [6]. The result is an efficient algorithm for full-wave extraction. For typical problems, IES³-based full-wave simulation is only about five times slower than IES³-based capacitance extraction for the same structure. We demonstrate the speed and accuracy of our approach by simulating an integrated inductor on a lossy CMOS substrate and comparing the results to measurement.

II. Formulation

For the purposes of this paper, we will assume a “two-and-a-half dimensional” setup, with thin conductors characterized by a surface conductivity σ . If we assume a time-harmonic steady-state solution, then in frequency domain, the electric field \mathbf{E} is expressed in terms of the vector potential \mathbf{A} and the scalar potential ϕ :

$$\mathbf{E}(\mathbf{r}) = \mathbf{E}_{\text{inc}}(\mathbf{r}) - j\omega\mathbf{A}(\mathbf{r}) - \nabla\phi(\mathbf{r}). \quad (1)$$

\mathbf{E}_{inc} is an incident (stimulus) field. The vector and scalar potentials are obtained by integrating over the conductor surfaces:

$$\mathbf{A}(\mathbf{r}) = \int_S \mathbf{G}^{\mathbf{A}}(\mathbf{r}, \mathbf{r}') \mathbf{J}(\mathbf{r}') dS', \quad (2)$$

and

$$\phi(\mathbf{r}) = \int_S G^{\phi}(\mathbf{r}, \mathbf{r}') \rho(\mathbf{r}') dS'. \quad (3)$$

\mathbf{J} is the surface current density, ρ is the surface charge density, $\mathbf{G}^{\mathbf{A}}$ is the (dyadic) vector potential Green’s function, and G^{ϕ} is the scalar potential Green’s function. In free space

$$\mathbf{G}^{\mathbf{A}}(\mathbf{r}, \mathbf{r}') = \frac{\mu_0}{4\pi} \frac{e^{-j\omega|\mathbf{r}-\mathbf{r}'|/c}}{|\mathbf{r}-\mathbf{r}'|} \mathbf{I} \quad (4)$$

$$G^{\phi}(\mathbf{r}, \mathbf{r}') = \frac{1}{4\pi\epsilon_0} \frac{e^{-j\omega|\mathbf{r}-\mathbf{r}'|/c}}{|\mathbf{r}-\mathbf{r}'|}, \quad (5)$$

where c is the speed of light and ϵ_0 and μ_0 are the permittivity and permeability of vacuum. In a layered medium, analytic expressions for the Green’s functions do not exist. However, there are a number of numerical approaches for computing them [7], [8], [14]. The layered media Green’s functions are briefly discussed in Section IV. The current density \mathbf{J} is related to the charge density ρ by

$$\nabla_S \cdot \mathbf{J}(\mathbf{r}) + j\omega\rho(\mathbf{r}) = 0. \quad (6)$$

At the surface of a conductor, the current density is given by $\mathbf{E} = \mathbf{J}/\sigma$. Combining this relation with Equation (1) yields

$$\frac{\mathbf{J}(\mathbf{r})}{\sigma} = \mathbf{E}_{\text{inc}}(\mathbf{r}) - j\omega\mathbf{A}(\mathbf{r}) - \nabla\phi(\mathbf{r}). \quad (7)$$

can be easily solved analytically. The resulting spectral-domain Green’s function must then be numerically transformed into space domain. Details of these procedures are involved and can be found in the microwave literature [1], [7], [8], [14].

We use the procedure described in [14] to efficiently compute these space domain Green’s functions. The results of the computation are tabulated in a database off-line. Building the database for a given process takes a few minutes. Evaluating a single interaction between a source and observation pair takes about twice as long as evaluating the free-space Green’s function for the pair.

V. Experimental Results

The simulator has been run on a number of examples, including capacitors, inductors, and filters on CMOS and MCM substrates. In this section, we report simulation results for an integrated inductor on a highly conductive CMOS substrate. The layout is shown in Figure 2. The inductor is constructed with the top two metal layers of the process.

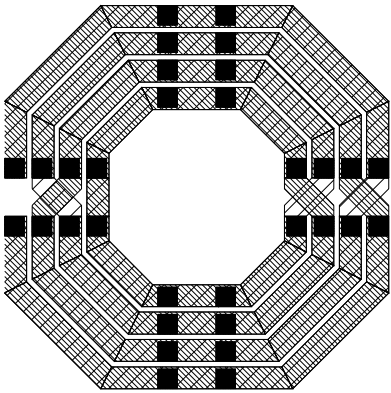


Fig. 2. CMOS inductor layout

For measurement purposes, the inductor was connected to a pad frame, and the same pad frame was included in the simulation to avoid uncertainties associated with de-embedding. The pads connected to one of the inductor terminals were grounded, and the single-port S parameter looking into the other pad was measured. This S parameter was converted into a complex impedance. Comparisons between the simulation results and measurement are shown in Figure 3. The graphs show the magnitude and phase of the complex impedance, and also the ratio of imaginary to real parts, which represents a quality factor Q for the inductor. The simulation predicts a slightly higher quality factor, but the discrepancy is well within the process variation. (Nominal values for all process parameters were used in the simulation.)

We also examined the performance of the simulator as the discretization level was increased. The results are shown in Figure 4. These simulations were of the inductor alone (no pads) for a single frequency of 3 GHz. Discretization sizes ranged from 1,500 elements to 11,500 elements, yielding matrix sizes of between 2,000 and 16,000 (the differ-

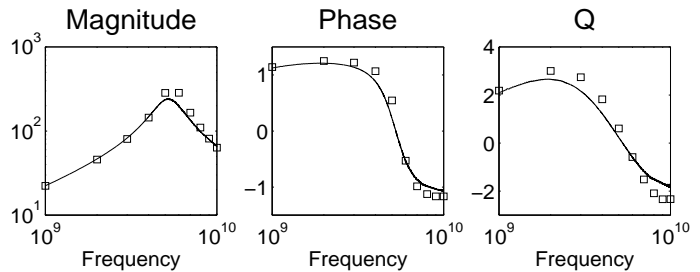


Fig. 3. Comparison of simulation (boxes) to measurement (lines)

ence is the number of divergence-free basis functions). The graphs show the total CPU time and the number of nonzeros in the compressed matrix representation. Both time and memory scale slightly faster than linearly as the system size grows. Almost all of the time goes into building the compressed matrix representation. The iterative solve, which is preconditioned using a sparse matrix that captures only the nearby interactions, required no more than thirty iterations at any discretization level to achieve a relative reduction of 10^4 in the norm of the residual. The smallest simulation took about four minutes, and the largest required about fifty minutes. The total simulation times compare favorably to the time required for extracting only the parasitic capacitance of the same inductor. At the highest discretization level, our IES³-based capacitance extractor [6] using the same Green’s functions requires ten minutes. Note that in the full-wave case, a triangle with three neighbors requires four integrals: one for computing the scalar potential, and one for each edge when computing the vector potential. Since each vector potential integral also involves manipulating vectors rather than scalars, the factor of five difference in time is about the best that can be expected.

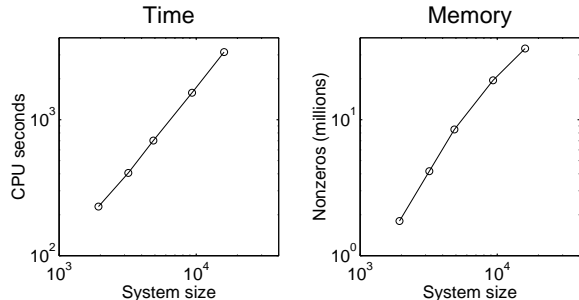


Fig. 4. Time and memory requirements

The convergence of Q (which is the most sensitive parameter computed from the simulation) as the discretization level is increased is shown in Figure 5. Low discretization levels tend to overestimate Q since current crowding effects are missed.

Results from the simulation can also be used to gain intuition about how the inductor is operating. The current distribution in one section of the inductor is shown in Figure 6. Light areas in the figure indicate higher current density. It is clear that significant current crowding occurs in the innermost turn.

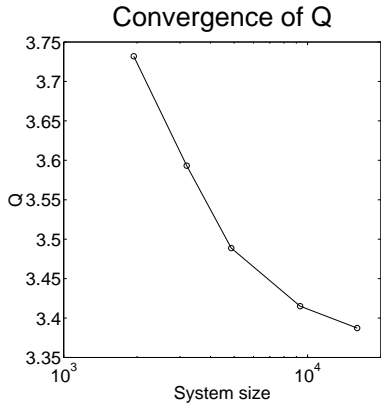


Fig. 5. Convergence behavior with increasing discretization

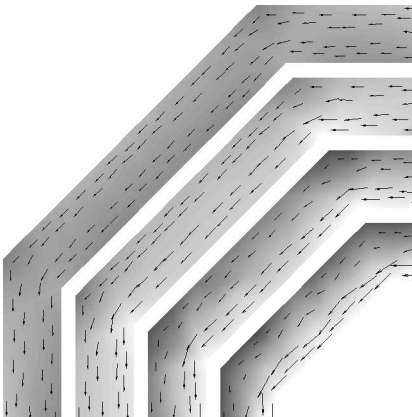


Fig. 6. Current flow in the inductor

Even though the simulation only solves for the current density in the conductors, we can use the layered Green's functions and Equation (1) to obtain the eddy currents that are induced in the conductive substrate. We do this by computing the substrate electric field arising from the conductor currents and then multiplying by the substrate conductivity. A cross section of the substrate together with the current density is shown in Figure 7. Nontrivial currents penetrate the substrate to depths on the order of one hundred microns.

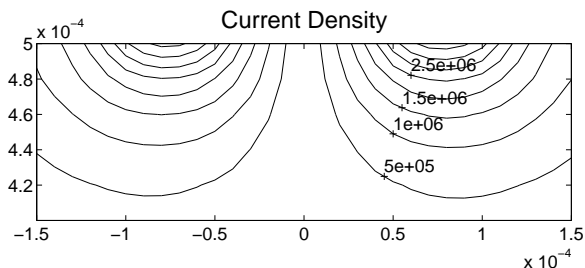


Fig. 7. Cross section of substrate showing eddy currents

VI. Conclusion

We described a general purpose full-wave electromagnetic analysis tool for the simulation of passive structures in layered, lossy media. The formulation is based on inte-

gral equations using layered Green's functions to capture the effects of the medium. The conductor current distribution is decomposed into curl-free and divergence-free parts in order to avoid ill-conditioning. An $O(N \log N)$ solution procedure is obtained by constructing and compressing the method-of-moments matrix using IES³ [6] together with an iterative solver. For typical problems, IES³-based full-wave simulation is only about five times slower than capacitance extraction for the same structure. Simulation results were presented for an integrated inductor on a lossy CMOS substrate. The results compare favorably to measurements.

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